



[2207/10554]

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of:

Examiner: Fred O. Ferris III

Yatin V. Hoskote et al.

For: SYSTEM AND METHOD FOR
AUTOMATICALLY MAPPING
STATE ELEMENTS FOR
EQUIVALENCE VERIFICATION

Filed: March 9, 2001

Serial No.: 09/802,616

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Art Unit 2128
I hereby certify that this correspondence is being deposited with the
United States Postal Service with sufficient postage as first class mail
in an envelope addressed to:
Mail Stop APPEAL BRIEF - PATENTS
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date: 4/21/2006

Signature: AARON C. DEDITCH

APPEAL BRIEF TRANSMITTAL

SIR:

Transmitted herewith for filing in the above-identified patent application, please find an Appeal Brief pursuant to 37 C.F.R. Part 41.37.

Please charge the Appeal Brief fee of \$500.00, and any other fees that may be required in connection with this communication to the deposit account of Kenyon & Kenyon LLP, deposit account number 11-0600.

Applicants hereby request a three-month extension of time for submitting the Appeal Brief. The extended period for submitting the Appeal Brief expires on April 21, 2006 (the Notice of Appeal was mailed on November 17, 2005, and filed in the Patent Office on November 21, 2005, which makes the three-month date January 21, 2006). Please charge the \$1,020.00 extension fee and any other fee that may be required to Deposit Account No. 11-0600. A duplicate of this Transmittal is enclosed.

Respectfully submitted,

Dated: 4/21/2006

By: Gerard A. Messina

Gerard A. Messina
Registration No. 35,952

04/28/2006 BABRAHA1 00000007 110600 09802616

02 FC:1253 1020.00 DA

KENYON & KENYON LLP
One Broadway
New York, NY 10004
(212) 425-7200
CUSTOMER NO. 26646



[02207/10554]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

-----X
In re Application of: : Examiner: Fred O. Ferris III
: :
Yatin V. Hoskote et al. : :
: :
For: SYSTEM AND METHOD FOR : :
AUTOMATICALLY MAPPING : :
STATE ELEMENTS FOR : :
EQUIVALENCE VERIFICATION : :
: :
Filed: March 9, 2001 : :
: Art Unit 2128
: :
Serial No.: 09/802,616 : :
: :
-----X

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

I hereby certify that this correspondence is being deposited with the
United States Postal Service with sufficient postage as first class mail
in an envelope addressed to:
Mail Stop APPEAL BRIEF - PATENTS
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
on
Date: 4/27/2006
Signature: AARON C. DEDITCH
(33,865)

APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

S I R:

In the above-identified patent application ("the present application"), the Appellants mailed a Notice of Appeal on November 17, 2005 from the Final Office Action issued by the United States Patent and Trademark Office on May 25, 2005. This Notice of Appeal was received by the Patent Office on November 21, 2005. Accordingly, the two month appeal date is January 21, 2006.

In the Final Office Action, claims 1 to 21 were finally rejected. An Advisory Action was mailed on September 1, 2005.

It is understood for purposes of the appeal that any Amendments to date have already been entered by the Examiner, and that the Response After Final does not require entry since it included no amendments.

04/28/2006 BABRAHA1 00000007 110600 09802616

01 FC:1402 500.00 DA

As to the length of the “concise explanation” of the subject matter defined in each of the claims involved in the appeal (see 41.37), the “concise explanation” language is like the “concise explanation” requirement of former Rule 37 C.F.R. § 1.192. Accordingly, the length of the concise explanation provided is therefore acceptable, since it would have been acceptable under 37 C.F.R. § 1.192 and since it specifically defines the subject matter of the independent claims involved in the appeal. In the filing of many appeal briefs under the old rule, the length of the “concise explanation” has always been accepted by the Patent Office.

It is therefore respectfully submitted that this Appeal Brief complies with 37 C.F.R. § 41.37. Although no longer required by the rules, this Brief is submitted in triplicate as a courtesy to the Appeals Board.

It is respectfully submitted that the final rejections of claims 1 to 21 should be reversed for the reasons set forth below.

1. REAL PARTY IN INTEREST

The real party in interest in the present appeal is Intel Corporation, 2200 Mission College Boulevard, P.O. Box 58119, Santa Clara, California, 95052-8119. Intel Corporation is the assignee of the entire right, title, and interest in the above-identified application.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences “which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.”

3. STATUS OF CLAIMS

Claims 1, 18 and 20 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,247,163 (“Burch”).

Claims 2 to 17, 19 and 21 stand finally rejected under 35 U.S.C. § 103(a) as being obvious over Burch in view of U.S. Patent No. 6,651,225 (“Lin”).

4. STATUS OF AMENDMENTS

In response to the Final Office Action issued on May 25, 2005, a Response was filed on August 9, 2005. The Response did not include any amendments to the claims.

It is understood for purposes of this appeal that any Amendments to date have already been entered by the Examiner, and that the Response After Final does not require entry since it included no amendments.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claims 1, 18 and 20 relate to a process for automatically mapping state elements between a first circuit and a second circuit.

FIG. 1 illustrates a high-level flow diagram of an embodiment of the automatic state element mapping process according to the present invention. The state element mapping method is divided into three phases: a structural phase (Phase 1) 10, an inversion detection phase (Phase 1.5) 20 and a functional phase (Phase 2) 30. As indicated by the arrows connecting the phases in FIG. 1, the phases are performed in sequential order and may be repeated depending upon whether a threshold criterion is satisfied, indicating that the mapping process is complete. (See page 3, line 29 to page 4, line 3).

During the structural phase, Phase 1, partial fanin signatures of state elements of a first specification circuit are compared to partial fanin signatures of state elements of a second implementation circuit. A fanin signature of a particular element includes an alphabetically sorted list of the primary inputs and other state elements which provide inputs to that state element. Comparison of fanout signatures between state elements is also performed, the fanout signatures including an alphabetically sorted list of primary outputs and other state elements to which a particular state element provides an output. In general, at the outset of the structural phase, fanin and fanout signatures will be incomplete because many of the input and output state elements have not yet been mapped and identified. Only mapped state elements are incorporated into the signatures, and therefore, the fanin and fanout signatures are largely 'partial' signatures. When only two state elements — one from each circuit — have a particular partial fanin or fanout signature, then the two elements are mapped to each other and given an identification. The structural phase increases the number of mapped elements in an iterative process in which fanin and fanout signatures are updated and made more complete when new mappings are identified, the updated signatures in turn leading to more mappings being identified. The process ends when no new mappings are identified or after a certain number of iterations during which no mappings are identified, referred to as the fix point. (See page 4, lines 5 to 25).

Generally, after the fix point has been reached, not all state elements have been mapped. Moreover, the mappings identified in the structural phase do not indicate whether the mappings are direct mapped, or inverse mapped, as they only indicate structural and not functional correspondence. Furthermore, due to the imperfect nature of attributing equivalence based solely on input and output structure, a small number of the mappings determined during the structural phase will be incorrect. Therefore, an inversion detection phase (Phase 1.5) is employed to determine the polarity (direct vs. inverse mapped status) of the mappings and to validate the mappings identified in the structural phase. (See page 4, line 27 to page 5, line 4).

However, prior to the commencement of the inversion detection phase, don't care conditions are identified, so that differences in output between two mapped state elements in response to these identified conditions does not cause their invalidation during the subsequent inversion detection and functional phases. After don't care conditions have been accounted for, the state elements mapped during the structural phase are fed random

input vectors on their respective inputs in a simulation. If the mapped state elements output the same values in response to equivalent input values, then they are direct mapped, and if they output opposite values they are inverse mapped. The inversion detection phase is also iterative, providing feedback via updates to the random simulation input vectors whenever a determination has been made. (See page 5, lines 5 to 16).

In FIG. 6, an exemplary inversion detection simulation is illustrated using mapped state elements U in the specification circuit 120 and V in the implementation circuit 122. In this exemplary illustration, both elements U and V have respective direct mapped inputs D and D', respective inverse mapped inputs L, L', respective mapped inputs M[1], M[1]' for which the polarity is undetermined, and unmapped inputs UM[2], UM[2]'. State elements U and V also have respective mapped outputs Z, Z' and two unmapped outputs UM[3], UM[4] and UM[3]', UM[4]'. (See page 9, line 28 to page 10, line 2).

The truth table 270 in FIG. 6 indicates the output values at Z, Z' for various combinations of input values at respective inputs D, D', L, L'. Each column has 32 rows (of which only several are shown), one for each bit of a 32-bit word. It is noted that D and D' have the same inputs in any given simulation, while L and L' have opposite inputs in any given simulation as they are inverse mapped. As shown, for each of the inputs, Z and Z' have exactly opposite-valued outputs, with one exception. In the row numbered 32, the set of inputs at D (=1), D' (=1), L (=0) and L' (=1) produce X values at the outputs Z, Z'. This result is a consequence of the undetermined elements, M[1], M[1]', UM[1], UM[1]' which affect the outputs Z, Z'. Due to the presence of the undetermined state elements (mapped and unmapped) the values at mapped outputs, such as Z, Z' can be indeterminate. However, having Xs at the output of Z, Z' does not invalidate the mapping, which, from the evidence that state elements U, V output opposite values at Z, Z' for each equivalent set of inputs, is determined to be an inverse mapping. If instead of having Xs for outputs for Z, Z' in row 32, the outputs at Z and Z' were both 1, the mapping would be invalidated because the consistent pattern of opposite valued outputs at Z, Z', indicating an inverse mapping relationship would be broken, demonstrating inconsistent functionality between state elements U and V. (See page 10, lines 4 to 20).

The inversion detection phase is also iterative in that mappings found in a stage are used to improve the input vectors fed in during subsequent stages to update the inputs and outputs of the various state element mappings. The completion of this stage

occurs in two instances: when the polarity of all known mappings has been determined, or, after a configurable number of iterations in which no further determinations are made. (See page 10, lines 22 to 26).

In summary, the presently claimed subject matter is directed to a method for automatically mapping state elements between a first circuit and a second circuit, the method including comparing, in a structural phase, structural features of state elements in the first circuit to structural features of state elements in the second circuit for equivalence, determining, during the structural phase, mappings between state elements of the first circuit and the second circuit based on the comparison of the structural features, accounting for don't care input conditions before comparing state element function, detecting, in an inversion detection phase, the polarity of the mappings, comparing, in a functional phase, the functionality of state elements in the first circuit to state elements in the second circuit for equivalence using a three-valued simulation, determining further mappings based upon the functional comparison during the functional phase, and detecting whether a threshold condition for completion of the mapping process is satisfied. (See claim 1).

Finally, the appealed claims include no means-plus-function language and no step-plus-function claims, so that 37 C.F.R. 41.37(v) is satisfied as to its specific requirements for such claims, since none are present here. Also, the present application does not contain any step-plus-function claims because the method claims in the present application are not "step plus function" claims because they do not recite "a step for", as required by the Federal Circuit and as stated in Section 2181 of the MPEP.

6. GROUND FOR REJECTIONS TO BE REVIEWED ON APPEAL

- A. Whether claims 1, 18 and 20 are anticipated by Burch.
- B. Whether claims 2 to 17, 19 and 21 are obvious over Burch in view of Lin.

7. ARGUMENTS

- A. **Claims 1, 18 and 20 are not anticipated by Burch.**

Claims 1, 18 and 20

Claims 1, 18 and 20 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by Burch. It is respectfully submitted that Burch does not anticipate claims 1, 18 and 20 for the following reasons.

In order for a claim to be anticipated under 35 U.S.C. § 102, a single prior art reference must disclose each and every element of the claim in exactly the same way. See Lindeman Maschinenfabrik v. Am. Hoist and Derrick, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

Independent claim 1 recites a method for automatically mapping state elements between a first circuit and a second circuit, the method including, *inter alia*, an ***inversion detection phase*** that detects whether the mappings are inverse mappings.

As discussed in the specification, an inversion detection phase is employed to determine the polarity (direct vs. inverse mapped status) of the mappings and to validate the mappings identified in the structural phase. (See page 5, lines 1 to 3). The Burch reference, by contrast, does not disclose (or even suggest) these features of claim 1.

The Final Office Action asserts that the Burch reference discloses these features in the logic discussion on cols. 3 to 5. However, this section does not, in fact, disclose detecting whether the mappings are ***inverse mappings***. Rather, this section defines the conditions for finding equivalence by semi-inductive predicates, but does not indicate or mention an inversion detection phase, in which inverse mappings are detected. Indeed, no such detection is mentioned, or even suggested, at all by Burch.

As to an inversion detection phase, the Final Office Action asserts that “Burch teaches a functionally equivalent process”, in particular, that col. 4, lines 57 to 67, of Burch disclose a purported refinement to the Burch mapping process that assumes both true and false latch output values, and that the polarity or opposite true/false value in any latch output would be inherently detected. It is respectfully submitted, however, that such assertions are unsupported, and moreover, do not demonstrate a disclosure of an inversion detection phase. In particular, col. 4, lines 57 to 67 do not refer to opposite or inverted mappings, as suggested by the Office, but rather merely to ***unequal latch states***. That is, col. 4, lines 57 to 67 simply refer to a state with respect to a particular latch l_0 as unequal to the state with respect to another latch l_1 . (See col. 5, lines 2 and 4, which makes reference to “ $S(l_0) \neq S(l_1)$ ”).

Moreover, such a reference to unequal latch states is made within the context of making a “***false assumption***” to prove by contradiction that if a certain latch mapping M_1 is a subset of another latch mapping M_0 , then for every state $P_{M_0}(S)$ implies $P_{M_1}(S)$. In

particular, it is assumed that there exists a state S such that $P_{M0}(S)$ is true and $P_{M1}(S)$ is false but such an assumption leads to the conclusion that if $P_{M1}(S)$ is false then there exists mapped latches with unequal states (e.g., $S(l_0) \neq S(l_1)$), which necessarily implies that $P_{M0}(S)$ must also be false, which contradicts the assumption that $P_{M0}(S)$ is true. Hence, the reference to unequal states between mapped latches l_0 and l_1 is merely part of a theoretical exercise to demonstrate that such unequal states cannot exist. Indeed, col. 4, lines 44 to 45 explicitly states the latches l_0 and l_1 are mapped together if and only if $M(l_0, l_1)$ is true. (See also col. 1, lines 65 to 66). Accordingly, it is respectfully submitted that such assertions by the Final Office Action with respect to col. 4, lines 57 to 67 are unsupported.

It is therefore respectfully submitted that Burch does not anticipate the subject matter of independent claim 1.

As independent claims 18 and 20 recite features analogous to those of claim 1, it is submitted that they are also not anticipated by the Burch reference for essentially the same reasons.

In view of the foregoing, reversal of the rejections of claims 1, 18 and 20 is respectfully requested.

B. Claims 2 to 17, 19 and 21 are not obvious over Burch in view of Lin.

Claims 2 to 17, 19 and 21

Claims 2 to 17, 19 and 21 stand finally rejected under 35 U.S.C. § 103(a) as being obvious over Burch in view of Lin. It is respectfully submitted that none of claims 2 to 17, 19 and 21 is obvious over Burch in view of Lin for at least the following reasons.

In order for a claim to be rejected for obviousness under 35 U.S.C. § 103(a), not only must the prior art teach or suggest each element of the claim, but the prior art must also suggest combining the elements in the manner contemplated by the claim. See *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934 (Fed. Cir. 1990), cert. denied, 111 S. Ct. 296 (1990); *In re Bond*, 910 F.2d 831, 834 (Fed. Cir. 1990). The Examiner bears the initial burden of establishing a prima facie case of obviousness. M.P.E.P. §2142. To establish a prima facie case of obviousness, the Examiner must show, inter alia, that there is some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references and that,

when so modified or combined, the prior art teaches or suggests all of the claim limitations. M.P.E.P. § 2143. Appellants respectfully submit that these criteria for obviousness are not met here.

First of all, the Lin reference does not mention or refer to inverse mappings at all, let alone detecting whether the mappings are inverse mappings. Accordingly, the Lin reference fails to cure the deficiencies of the primary Burch reference discussed above with respect to claims 1, 18 and 20, and therefore, for this reason alone, the combination of Burch and Lin does not render obvious independent claims 1, 18 and 20, or their respective dependent claims 2 to 17, 19 and 21.

Moreover, the Final Office Action's assertion that “a skilled artisan would have made an effort to become aware of what capabilities had been developed in the market place, and hence, would have knowingly modified Burch with the teachings of Lin” is mere hindsight reasoning and fails to demonstrate a requisite motivation to modify the Burch reference to provide the claimed features, which the Office Action admits is not disclosed by Burch. Indeed, the Final Office provides no motivation whatsoever, except to say that “[a]n obvious motivation exists since this area of technology is highly competitive with many types of equivalence verification process available for VSLI circuit development in the market place and large amounts of money being spent in product development and improvement.” Accordingly, there is no credible support to modify Burch in the manner contemplated by the assertions of the Final Office Action.

In this regard, the cases of In re Fine, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988), and In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992), make plain that the Final Office Action's generalized assertions that it would have been obvious to modify the references relied upon do not properly support a § 103 rejection. It is respectfully suggested that those cases make plain that the Final Office Action reflects a subjective “obvious to try” standard, and therefore does not reflect the proper evidence to support an obviousness rejection based on the references relied upon.

Moreover, the “problem confronted by the inventor must be considered in determining whether it would have been obvious to combine the references in order to solve the problem.” (See Diversitech Corp. v. Century Steps, Inc., 850 F.2d 675, 679 (Fed. Cir. 1998)). It is respectfully submitted that, as discussed above, the references relied on, whether taken alone or combined, do not suggest in any way modifying or combining the

references so as to provide the presently claimed subject matter for addressing the problems and/or providing the benefits of the claimed subject matter, including, for example, a method for automatically mapping state elements between a first circuit and a second circuit, which includes an *inversion detection phase* that detects whether the mappings are inverse mappings, as explained herein and in the specification.

As further regards all of the obviousness rejections of the claims, it is respectfully submitted that not even a *prima facie* case has been made in the present case for obviousness, since the Office Actions to date never made any findings, such as, for example, regarding in any way whatsoever what a person having ordinary skill in the art would have been at the time the claimed subject matter of the present application was made. (See *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998) (the “factual predicates underlying” a *prima facie* “obviousness determination include the scope and content of the prior art, the differences between the prior art and the claimed invention, and the level of ordinary skill in the art”)). It is respectfully submitted that the proper test for showing obviousness is what the “combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art”, and that the Patent Office must provide particular findings in this regard — the evidence for which does not include “broad conclusory statements standing alone”. (See *In re Kotzab*, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir. 2000) (citing *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1618 (Fed. Cir. 1999) (obviousness rejections reversed where no findings were made “concerning the identification of the relevant art”, the “level of ordinary skill in the art” or “the nature of the problem to be solved”))). It is respectfully submitted that there has been no such showings by the Office Actions to date or by the Advisory Action.

In fact, the present lack of any of the required factual findings forces both Appellant and this Board to resort to unwarranted speculation to ascertain exactly what facts underly the present obviousness rejections. The law mandates that the allocation of the proof burdens requires that the Patent Office provide the factual basis for rejecting a patent application under 35 U.S.C. § 103. (See *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d 1011, 1016, 154 U.S.P.Q. 173, 177 (C.C.P.A. 1967))). In short, the Examiner bears the initial burden of presenting a proper *prima facie* unpatentability case — which has not been met in the present case. (See *In re Oetiker*, 977 F.2d 1443, 1445, 24, U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992)).

Accordingly, for at least these further reasons, it is respectfully submitted that Burch in view of Lin does not render claims 2 to 17, 19 and 21 obvious.

In view of the foregoing, reversal of the rejections of claims 2 to 17, 19 and 21 is respectfully requested.

In view of the above, it is respectfully requested that the rejections of claims 1 to 21 be reversed, and that these claims be allowed as presented.

Dated: 4/21/2006

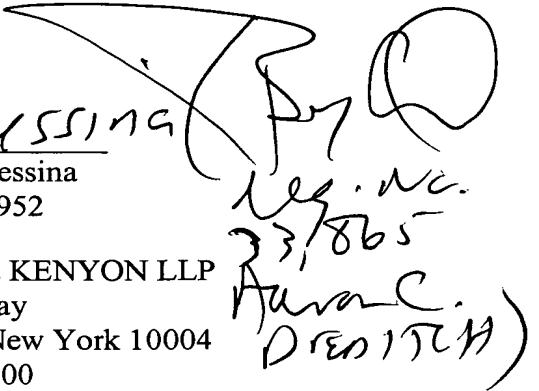
Respectfully submitted,

By: 

Gerard A. Messina
Reg. No. 35,952

KENYON & KENYON LLP
One Broadway
New York, New York 10004
(212) 425-7200

CUSTOMER NO. 26646


Reg. No.
33,865
Hara C.
DRENITIA

CLAIMS APPENDIX

1. A method for automatically mapping state elements between a first circuit and a second circuit, comprising:

- a) comparing, in a structural phase, structural features of state elements in the first circuit to structural features of state elements in the second circuit for equivalence;
- b) determining, during the structural phase, mappings between state elements of the first circuit and the second circuit based on the comparison of the structural features;
- c) accounting for don't care input conditions before comparing state element function;
- d) detecting, in an inversion detection phase, the polarity of the mappings;
- e) comparing, in a functional phase, the functionality of state elements in the first circuit to state elements in the second circuit for equivalence using a three-valued simulation;
- f) determining further mappings based upon the functional comparison during the functional phase; and
- g) detecting whether a threshold condition for completion of the mapping process is satisfied.

2. The method of claim 1, further comprising:

- h) building, in the structural phase, initial fanin and fanout partial signatures for each state element in the first and second circuits;
- i) determining whether at least one of a fanin partial signature and a fanout partial signature for a first unmapped state element in the first circuit is equivalent to a respective one of a fanin partial signature and a fanout partial signature of a second unmapped state element of the second circuit;
- j) further determining if the first state element and the second state element are the only state elements which share an equivalent at least one of a fanin partial signature and fanout partial signature; and
- k) mapping the first and second state elements to one another if it is determined that they are the only state elements which share the at least one of the fanin partial signature and fanout partial signature.

3. The method of claim 2, further comprising:

- l) updating the fanin and fanout partial signatures of the state elements of the first and second circuits based on the mapping between the first and second state elements.

4. The method of claim 3, further comprising:

repeating steps i) through l) until a fix point is reached ending the structural phase, the fix point occurring at a completion of a number of repeated iterations during which no further mappings are determined.

5. The method of claim 2, wherein the fanin partial signature is a list of mapped inputs to the state element, and the fanout partial signature is an alphabetically sorted list of mapped outputs from the state element.

6. The method of claim 1, further comprising:

m) inputting random values, excluding don't care conditions, to each element of a pair of mapped state elements during the inversion detection phase, the random values being bit values for mapped inputs having a known polarity and being a third value for unmapped inputs and mapped inputs having an unknown polarity;

n) comparing output values from each element of the pair of state elements based on the input random values; and

o) determining whether the pair is one of direct and inverse mapped based on the comparison.

7. The method of claim 6, wherein the mapped inputs to each element of the pair of elements having a known polarity are one of direct mapped inputs and inverse mapped inputs, direct mapped inputs to each element being provided with equivalent random values, inverse mapped inputs to each element being provided with complementary random values.

8. The method of claim 7, further comprising:

p) updating the fanin and fanout partial signatures of the state elements of the first and second circuits to reflect the determination of polarity for the pair of state elements.

9. The method of claim 6, further comprising:

q) validating the mapping of the pair of state elements if the comparison indicates that the mapping is one of a direct mapping and an inverse mapping.

10. The method of claim 6, further comprising:

simulating parallel versions of a pair of mapped state elements;

making parallel comparisons of the parallel versions; and

determining whether the pair is one of direct and inverse mapped based on the comparisons of the parallel versions.

11. The method of claim 10, wherein 32 parallel version are simulated using 32-bit panel simulation.

12. The method of claim 8, further comprising:

repeating steps m) through q) until an inversion fix point is reached ending the inversion detection phase, the inversion fix point occurring after completion of a number of repeated iterations during which no further polarity determinations are made.

13. The method of claim 12, further comprising:

r) grouping, in the functional phase, all unmapped state elements in an initial class;
s) inputting equivalent random values to each of the unmapped state elements; and
t) refining the unmapped state elements into equivalence classes based upon at least one of an equivalent output property and a precisely opposite output property generated in response to the input random values.

14. The method of claim 12, wherein random bit values are input to mapped inputs and a third value is input to unmapped inputs.

15. The method of claim 13, further comprising:

u) determining equivalence classes which include two state elements, one state element being from each of the first and second circuits;

v) mapping the two state elements in the determined equivalence classes to one another; and

w) updating the fanin and fanout partial signatures of the state elements of the first and second circuits based on the mapping between the two state elements.

16. The method of claim 15, further comprising:

repeating steps s) through w) until a functional fix point is reached, the functional fix point occurring after a completion of one of:

I) a number of repeated iterations during which no further mappings are determined; and

II) a mapping of all state elements of the first and second circuits;

and

outputting mappings and equivalence classes.

17. The method of claim 1, further comprising:

comparing, in a second structural phase, structural features of state elements in the first circuit to structural features of state elements in the second circuit for equivalence;

determining, during the second structural phase, mappings between state elements of the first circuit and the second circuit based on the comparison of the structural features;

detecting, in a second inversion detection phase, the polarity of the mappings; and

outputting final mappings as a function of the detection;

wherein, in each phase, results from all previous phases are used to improve inputs.

18. An article comprising a computer-readable medium which stores computer-executable instructions for causing a computer system to:

compare, in a structural phase, structural features of state elements in the first circuit to structural features of state elements in the second circuit for equivalence;

determine, during the structural phase, mappings between state elements of the first circuit and the second circuit based on the comparison of the structural features;

account for don't care input conditions before comparing state element function;

detect, in an inversion detection phase, the polarity of the mappings;

compare, in a functional phase, the functionality of state elements in the first circuit to state elements in the second circuit for equivalence using a three-valued simulation;

determine further mappings based upon the functional comparison during the functional phase; and

detect whether a threshold condition for completion of the mapping process is satisfied.

19. The article of claim 18 which further stores instructions causing a computer system to:

input random values to each element of a pair of mapped state elements during the inversion detection phase, the random values being bit values for mapped inputs having a known polarity and being a third value for unmapped inputs and mapped inputs having an unknown polarity;

compare output values from each element of the pair of state elements based on the input random values; and

determine whether the pair is one of direct and inverse mapped based on the comparison.

20. A computer system for automatically mapping state elements between a first circuit and a second circuit, comprising:

an input interface; and

a processor, the processor configured to:

compare, in a structural phase, structural features of state elements in the first circuit to structural features of state elements in the second circuit for equivalence;

determine, during the structural phase, mappings between state elements of the first circuit and the second circuit based on the comparison of the structural features;

account for don't care input conditions specified using the input interface before comparing state element function;

detect, in an inversion detection phase, the polarity of the mappings;

compare, in a functional phase, the functionality of state elements in the first circuit to state elements in the second circuit for equivalence using a three-valued simulation;

determine further mappings based upon the functional comparison during the functional phase; and

detect whether a threshold condition for completion of the mapping process is satisfied.

21. The computer system of claim 20, wherein the processor is further configured to:

input random values to each element of a pair of mapped state elements during the inversion detection phase, the random values being bit values for mapped inputs having a known polarity and being a third value for unmapped inputs and mapped inputs having an unknown polarity;

compare output values from each element of the pair of state elements based on the input random values; and

determine whether the pair is one of direct and inverse mapped based on the comparison.

U.S. Application Serial No. 09/802,616
Attorney Docket No.: 2207/10554
Appeal Brief

EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132. No other evidence has been entered by the Examiner or relied upon by Appellant in the appeal.

RELATED PROCEEDINGS APPENDIX

As indicated above in Section 2 of this Appeal Brief, “[t]here are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellant or the assignee, Intel Corporation, ‘which may be related to, directly affect or be directly affected by or have a bearing on the Board’s decision in the pending appeal.’ ” As such, there are no “decisions rendered by a court or the Board in any proceeding identified pursuant to [37 C.F.R. § 41.37(c)(1)(ii)]” to be submitted.